

CLAIMS

What is claimed is:

1 1. A decoupling capacitor for a semiconductor device, said capacitor
2 comprising:
3 a first low dielectric insulator layer;
4 a low resistance conductor formed into at least two interdigitized
5 patterns on a surface of the first low dielectric insulator layer, each of said two
6 interdigitized patterns being adjacent the other such that their sidewalls form
7 plates of said capacitor; and
8 a high dielectric material provided between said two interdigitized
9 patterns.

1 2. The decoupling capacitor of claim 1, wherein said high dielectric
2 material comprises tantalum pentoxide.

1 3. The decoupling capacitor of claim 1, wherein said high dielectric
2 material comprises silicon nitride.

1 4. The decoupling capacitor of claim 1, further comprising a second
2 low dielectric insulator layer provided on said high dielectric material and said
3 interdigitized patterns.

1 5. The decoupling capacitor of claim 1, further comprising a polish
2 stop provided on each of said two interdigitized patterns.

1 6. The decoupling capacitor of claim 5, wherein said polish stop
2 comprises diamond-like carbon.

1 7. The decoupling capacitor of claim 5, wherein said polish stop is
2 non-conformally deposited on said interdigitized patterns.

1 8. The decoupling capacitor of claim 5, wherein said polish stop
2 comprises silicon nitride.

1 9. The decoupling capacitor of claim 1, wherein said first low
2 dielectric insulator layer comprises fluorinated glass.

1 10. A capacitor for a semiconductor device, said capacitor comprising:
2 a first low dielectric layer;
3 a plurality of interdigitized metal wires provided on said first low
4 dielectric layer;
5 high dielectric material provided between said plurality of
6 interdigitized metal wires; and

7 a second low dielectric layer provided on said high dielectric
8 material.

1 11. The capacitor of claim 10, wherein said high dielectric material
2 comprises tantalum pentoxide.

1 12. The capacitor of claim 10, wherein said high dielectric material
2 comprises silicon nitride.

1 13. The capacitor of claim 10, further comprising a polish stop
2 provided on each of the plurality of interdigitized metal wires.

1 14. The capacitor of claim 13, wherein said polish stop comprises
2 diamond-like carbon.

1 15. The capacitor of claim 13, wherein said polish stop is non-
2 conformally deposited on said plurality of interdigitized metal wires.

1 16. The capacitor of claim 13, wherein said polish stop comprises
2 silicon nitride.

1 17. A method of manufacturing a capacitor, the method comprising:
2 forming interdigitized metal wires on a first low dielectric material;
3 depositing a high dielectric material between each of said
4 interdigitized metal wires; and
5 depositing a second low dielectric material on said high dielectric
6 material such that said interdigitized metal wires are provided between said first
7 and second low dielectric material.

1 18. The method of claim 17, further comprising depositing polish stop
2 material at least on said metal wires prior to depositing said high dielectric
3 material.

1 19. The method of claim 17, wherein said polish stop is also deposited
2 on said first low dielectric material between said interdigitized metal wires.

1 20. The method of claim 19, further comprising etching back said high
2 dielectric material at least to a top surface of said interdigitized metal wires.

1 21. A method of manufacturing a capacitor, the method comprising:
2 depositing high dielectric material on a first low dielectric material;
3 etching a trough region in said high dielectric material;

4 filling said trough region with metal; and
5 depositing second low dielectric material on said trough region
6 filled with said metal and said high dielectric material.

1 22. The method of claim 21, further comprising depositing an etch stop
2 layer on said first low dielectric material such that said etch stop layer is between
3 said high dielectric material and said first low dielectric material.

1 23. The method of claim 22, further comprising removing said etch
2 stop layer from areas within said trough region after etching said trough and prior
3 to filling said trough region with said metal.

1 24. A circuit for monitoring a plurality of capacitor segments, the
2 circuit comprising:
3 a charge monitoring circuit coupled to each capacitor segment;
4 a coupling circuit for selectively coupling and decoupling one of
5 said capacitor segments from among a plurality of states; and
6 a control circuit for sequentially controlling said coupling circuit of
7 each of said capacitor segments so as to disconnect a failed capacitor segment
8 while said other capacitor segments are monitored.

1 25. The circuit of claim 24, wherein each of said capacitor segments
2 comprises a plurality of plates and wherein said coupling circuit comprises at least
3 one n-channel transistor connected between said control circuit and a plate of said
4 capacitor segment.

1 26. The circuit of claim 25, further comprising a fuse circuit provided
2 between said capacitor segment and said at least one n-channel transistor.

1 27. The circuit of claim 24, wherein each of said capacitor segments
2 comprises a plurality of plates and wherein said coupling circuit comprises at least
3 one p-channel transistor connected between said control circuit and a plate of said
4 capacitor segment, the other plate of the capacitor segment being connected to a
5 ground potential.

1 28. The circuit of claim 27, wherein said coupling circuit further
2 comprises a fuse circuit connected between said control circuit and said at least
3 one p-channel transistor.

1 29. The circuit of claim 24, wherein said charge monitoring circuit
2 outputs a signal based on an amount of current flowing through said capacitor
3 segment when said coupling segment is in a test state.

1 30. The circuit of claim 24, wherein said charge monitoring circuit
2 comprises an integrator circuit.

1 31. The circuit of claim 24, wherein the control circuit controls the
2 coupling circuit such that the capacitor segment is disconnected only after failing
3 at least twice.

1 32. A circuit for monitoring a plurality of capacitor segments, each
2 capacitor segment comprising a first low dielectric insulator layer, a low
3 resistance conductor formed into at least two interdigitized patterns on a surface
4 of said first low dielectric insulator layer and high dielectric material provided
5 between said two interdigitized patterns, the circuit comprising:
6 a charge monitoring circuit coupled to each of said capacitor
7 segments;
8 a coupling circuit connected to each of said capacitor segments,
9 said coupling circuit selectively coupling and decoupling each capacitor segment
10 to one of a disabled state, an enabled state and a testing state; and
11 a control circuit connected to said coupling circuit, said control
12 circuit controlling said coupling circuit so as to place said coupling circuit of a

13 failed capacitor in the disabled state while monitoring remaining ones of said
14 plurality of capacitor segments.

1 33. The circuit of claim 32, wherein each of said capacitor segments
2 comprises a plurality of plates and wherein said coupling circuit comprises at least
3 one n-channel transistor connected between said control circuit and a plate of said
4 capacitor segment.

1 34. The circuit of claim 33, further comprising a fuse circuit provided
2 between said capacitor segment and said at least one n-channel transistor.

1 35. The circuit of claim 32, wherein each of said capacitor segments
2 comprises a plurality of plates and wherein said coupling circuit comprises at least
3 one p-channel transistor connected between said control circuit and a plate of said
4 capacitor segment, the other plate of said capacitor segment being connected to a
5 ground potential.

1 36. The circuit of claim 35, wherein the coupling circuit further
2 comprises a fuse circuit connected between said control circuit and said at least
3 one p-channel transistor.

1 37. The circuit of claim 32, wherein said charge monitoring circuit
2 outputs a signal based on an amount of current flowing through said capacitor
3 segment when said coupling segment is in the testing state.

1 38. The circuit of claim 32, wherein said charge monitoring circuit
2 comprises an integrator circuit.

1 39. The circuit of claim 32, wherein the control circuit controls the
2 coupling circuit such that the failed capacitor segment is placed in the disabled
3 state only after failing at least twice in the testing state.